Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-20. (Canceled)

21. (Previously amended) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate;

at least one second well of the first conductivity type formed in at least one first well; and

at least one third well of the second conductivity type formed in at least one first well, wherein

the semiconductor device is composed of semiconductor circuits each formed in at least one first well, at least one second well and at least one third well.

22-27. (Canceled)

28. (Previously added) The semiconductor device according to claim 21, wherein potentials different from each other are supplied to the first and second wells.

29-34. (Canceled)

35. (Previously added) The semiconductor device according to claim 21, wherein potentials different from each other are supplied to the first, second and third wells.

36-41. (Canceled)

42. (Currently amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

a second well region of the first conductivity type formed in each of the at least two first well regions; and

integrated circuits which are formed on the at least two first well regions and the second well region, respectively, and which have different functions ~~.~~

wherein the second well region of the first conductivity type having a third well region of the second conductivity type formed therein, formed in each of the at least two first well regions and one of the integrated circuits formed in the each of the at least two first well region, the second well region and the third well region.

43. (Previously amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

a second well region of the first conductivity type formed in each of the at least two first well regions;

a third well region of the second conductivity type formed in each of the at least two first well regions; and

the integrated circuits formed on each of the at least two first well regions, the second well region and the third well region.

44-45. (Canceled)

46. (Previously added) The semiconductor integrated circuit device according to claim 42, wherein a potential is supplied to the at least two first well regions.

47. (Previously amended) The semiconductor integrated circuit device according to claim 43, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region and the third well region.

48. (Currently amended) The semiconductor integrated circuit device according to claim ~~44~~ 42, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region.

49. (Currently amended) The semiconductor integrated circuit device according to claim ~~42~~ 43, wherein at least one of the integrated circuits is one of a non-volatile memory circuit, an analog circuit, a digital circuit, a digital/analog

circuit, a static memory circuit, a random-access memory circuit, and a processor circuit.

50. (Previously added) The semiconductor integrated circuit device according to claim 49, wherein each of the integrated circuits has a potential application terminal for receiving a different potential applied thereto.

51. (Previously added) The semiconductor integrated circuit device according to claim 50, wherein each of the integrated circuits has a dedicated output terminal for outputting an output signal when the potential is applied to the potential application terminal thereof.

52. (Previously added) The semiconductor integrated circuit device according to claim 51, wherein each of the integrated circuits includes a control circuit for performing on/off control of application of the potential to the potential application terminal thereof.

53. (Previously added) The semiconductor integrated circuit device according to claim 52, wherein each of the integrated circuits includes a voltage generating circuit for application of the potential to the potential application terminal thereof.

54. (Previously added) The semiconductor integrated circuit device according to claim 42, further comprising:

a bias wiring system for supplying a bias potential to the semiconductor substrate; and

a power supply wiring system for supplying operation power to the integrated circuits,

wherein the bias wiring system and the power supply wiring system are located such that the bias wiring system and the power supply wiring system are independent of and not connected to each other.

55. (Previously amended) The semiconductor integrated circuit device according to claim 43, wherein a back gate bias is supplied to the at least two first well regions, the second well region and the third well region, and an input/output circuit or an interface circuit is formed in the at least two first well regions, the second well regions and the third well region.

56-61. (Canceled)

62-67. (Withdrawn)